REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-16, 18 and 22 are in the case. No amendments have been made.

Applicants acknowledge with appreciation the allowance of Claims 1 – 16.

Regarding the rejection of Claims 18 and 22 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Park et al. in view of Bernstein et al., this rejection is respectfully traversed. The patent to Park et al. was discussed in the previous Amendment, filed June 5, 2003. Such discussion is hereby incorporated by reference as if it were set forth in its entirety in this paragraph.

The patent to Bernstein et al. fails to cure the deficiencies of the patent to Park et al. Thus, unlike the invention as set forth in Claims 18 and 22, the patent to Park et al. apparently relates to a dynamic threshold metal oxide semiconductor (DTCMOS) circuits having features that allegedly can improve the speed performance of such circuits. Specifically, Bernstein et al. make use of a body contract for controlling the voltage threshold of a device which receives a logic signal. n earlier arriving logic signal is coupled to the gate of one input transistor, as well as to the body contact of another transistor receiving a later arriving logic signal. A data transition on the earlier arriving logic signal allegedly lowers the voltage threshold of the input transistor receiving the later arriving signal, thus dynamic lowering the voltage threshold, and thereby permitting an increase in speed for the logic circuit. This is unlike the purpose or function of the invention as set forth in both Claim 18 and Claim 22. Rather, their purpose and function is an improved ESD structure.

Significantly, Bernstein et al. do not show or suggest an input pad connected to the gate of a first transistor and to the drain of a second transistor. Nor is there any suggestion or even motivation for them to do so, as the purpose

of their circuits is different from the purpose of the circuit as claimed in Claim 18 and Claim 22, as discussed above.

Now, it was alleged in the above-identified Office Action that "Bernstein discloses in figure 4, a two input NAND gate which uses two transistors 41 and 42, such that the pad A (actually, input terminal 39) is connected to the gate of the first transistor, 42, and the drain of the second transistor, 41." However, a close inspection of such figure 4 reveals that no connection is made by their pad A to the drain of transistor 41, nor, indeed to the drain of any transistor. Note that connections of visually intersecting wire lines are depicted in such figure 4, and, indeed, in all of the Bernstein et al. circuit diagrams, as a large dot. Where no such large dot is shown at a wire visual intersection there is no electrical connection. Note, for example, the large dot at the intersection of a first wire connected to pad A and proceeding vertically upward and a second wire connected to the gate of transistor 41. Note also that there is no such dot where the first wire intersects a third wire connecting the drain of transistor to Vdd. Rather, the second wire continues to the body contact of transistor 41, it merely having in the figure to cross over, as it were, the third wire to get to such body contact. Note that if a mere visual intersection indicated an electrical connection, then in such figure 4 pad B (i.e., input terminal 40) would be connected to ground. Since pad B is an input terminal, that makes no sense, and would negate the discussion at, for example, column 2, lines 43-65, of the Bernstein et al. patent.

The other art of record is even less relevant.

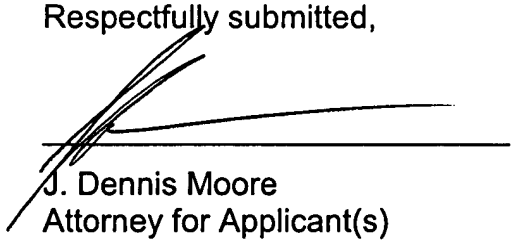
It is therefore respectfully submitted that neither Park et al., nor Bernstein et al., nor, indeed, any of the art of record show or suggest the invention as set forth in Claim 18 and Claim 22, whether considered alone or in any combination, and that therefore Claim 18 and Claim 22 are patentable over all of the art of record. Wherefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



J. Dennis Moore
Attorney for Applicant(s)
Reg. No. 28,885

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
Phone: (972) 917-5646
Fax: (972) 917-4418